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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,399	12/11/2003	Teruyuki Maeda	60437 (70820)	2109

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EXAMINER	
PHAM, LONG	

ART UNIT	PAPER NUMBER
2814	

MAIL DATE	DELIVERY MODE
07/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/735,399	MAEDA, TERUYUKI	
	Examiner	Art Unit	
	Long Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 3, 4, 6, and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Hutter et al. (US pat 5455447).

With respect to claim 1, Hutter et al. teach a power transistor comprising (see figs. 4 and 5 and associated text and claims 1-3):

a plurality of vertical PNP transistors (see claims 1-3) formed on a P-type silicon substrate 48 ,

an N+ type buried layer 82 formed to isolate the P-type silicon substrate and the plurality of vertical PNP transistors from each other, and

at least one electrode portion of N+ type buried layer, which has an N+ type diffusion layer 56,50 contacting the N+ type buried layer, wherein

the at least one electrode portion is located in an active region of the power transistor surrounded from all around by the vertical PNP transistors (since Hutter et al. teach forming a plurality of vertical pnp transistors, one pnp transistor would be surrounded by other pnp transistors).

With respect to claim 2, Hutter et al. further teach at least part of the electrode portion is provided under common emitter metal lines of the power

transistor routed on the active region of the power transistor. See figs. 4 and 5 and associated text and claims 1-3.

With respect to claim 3, Hutter et al. further teach the at least one electrode portion is provided on the N+ type buried layer and formed of an N+ type electrode layer 56b for making ohmic contact (with metal if metal is present) and an N+diffusion layer 50c. See figs. 4 and 5 and associated text and claims 1-3.

With respect to claim 4, Hutter et al. further an N+ type base well layer 54 as a base region of the plurality of vertical PNP transistors. Further how the N+type diffusion layer and the base region are formed has not been given patentable weight since claimed invention is directed to a device. See figs. 4 and 5 and associated text and claims 1-3.

With respect to claim 6, Hutter et al. further teach the N+type diffusion layer reaches the N+ type buried layer present on a bottom face of the power transistor. Further, how the N+type diffusion layer reaches the N+ type buried layer has not been given patentable weight since claimed invention is directed to a device.

With respect to claim 8, Hutter et al. further teach the power transistor as defined in claim 1.

Claim 9 is rejected under 35 U.S.C. 102(b) as being anticipated by Hutter et al. (US pat 5455447).

With respect to claim 9, Hutter et al. teach a power transistor having suppression of problematic leak current, the power transistor comprising (see figs. 4 and 5 and associated text and claims 1-3):

a plurality of vertical PNP transistors formed on a P-type substrate, each PNP transistor having a P+ type collector 86, an N+ type base well 54c formed at a base region, a P+ type emitter layer 64e and an N+ type base layer 54c;

P+ type collector buried layers 84 formed under the N+ type base well;

an N+ type buried layer 82 isolating the P-type substrate from the P+ type collector;

an N- type layer 54c formed over a surface of the P-type substrate;

an N+ type electrode layer 56b ; and

a plurality of N+ type diffusion layers 50c at electrode portions 56b within an active region under, contacting and surrounding (because of the plurality of pnp transistors) the N+ type electrode layer to reduce resistance of the N-type layer by extending therethrough to contact the N+ type buried layer, wherein at least one of the N+ type diffusion layers passes between the P+ type collector buried layers (because of the plurality of pnp transistors).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hutter et al. (US pat 5455447).

With respect to claim 5, Hutter et al. further teach an N type layer 54c formed on the P-type silicon substrate but fail to teach the relative concentration for the N+type diffusion layer.

However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value or range

for the relative concentration for the N+type diffusion layer through routine experimentation and optimization to obtain optimal or desired device performance because absence any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

With respect to claim 7, Hutter et al. also fail to teach the relative distance between the one electrode portion and adjacent electrode portions.

However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value or range for the relative concentration for the relative distance between the one electrode portion and adjacent electrode portions through routine experimentation and optimization to obtain optimal or desired device performance because absence any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

Response to Arguments

Applicant's arguments with respect to claims 1-9 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 571-272-1714. The examiner can normally be reached on Mon-Frid, 10am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Long Pham
Primary Examiner
Art Unit 2814

LP